

Brain Imaging Device, Drive Circuitry

PROJECT PLAN

Team DEC1619

Advisor/Client - Dr. Bigelow

Miguel Mondragon - Team Leader

Honghao Liu - Key Concept Holder

Zechariah Pettit - Webmaster

Team Email - DEC1619@iastate.edu

Team Website

Revised: 4/22/2016, Version 3

Contents

1 Introduction

1.1 Project statement

1.2 purpose

1.3 Goals

2 Deliverables

3 Design

3.1 Previous work/literature

3.2 Proposed System Block diagram

3.3 Assessment of Proposed methods

3.4 Validation

4 Project Requirements/Specifications

4.1 functional

4.2 Non-functional

5 Challenges

6 Timeline

6.1 First Semester

6.2 Second Semester

7 Conclusions

8 References

9 Appendices

1 Introduction

1.1 PROJECT STATEMENT

This project is to create the drive circuitry to a brain scanning device. The device requires the splitting of high frequency digital input signals into two lower frequency signals with individual phase control. These digital signals then will be sampled using a digital to analog converter then it need to be filtered and amplified in accordance with design goals set forth by our advisor. These signals will then be sent further on for functions relating to brain imaging in a portion of the device not covered by this project.

1.2 PURPOSE

The main purpose of this device is to provide a more mobile and possibly cost effective method for accurate brain imaging as seen in devices such as an MRI. Provided the device is capable of performing the functions set forth by the advisor it will provide a method for accurate imaging with the potential for wearability allowing for scanning during things such as exercise, sleep, and everyday life.

1.3 GOALS

The goals of this design and the project as a whole are as follows.

- Provide accurate phase control to output signals.
- Allow for considerable power amplification while ensuring a stable device.
- Limited noise in spite of the device's high frequency signals.
- Conversion from a digital input signal into several analog output signals.
- Final version of project presented on a PCB board.

2 Deliverables

Circuit Schematic detailing all aspects, parts, and outputs of the design.

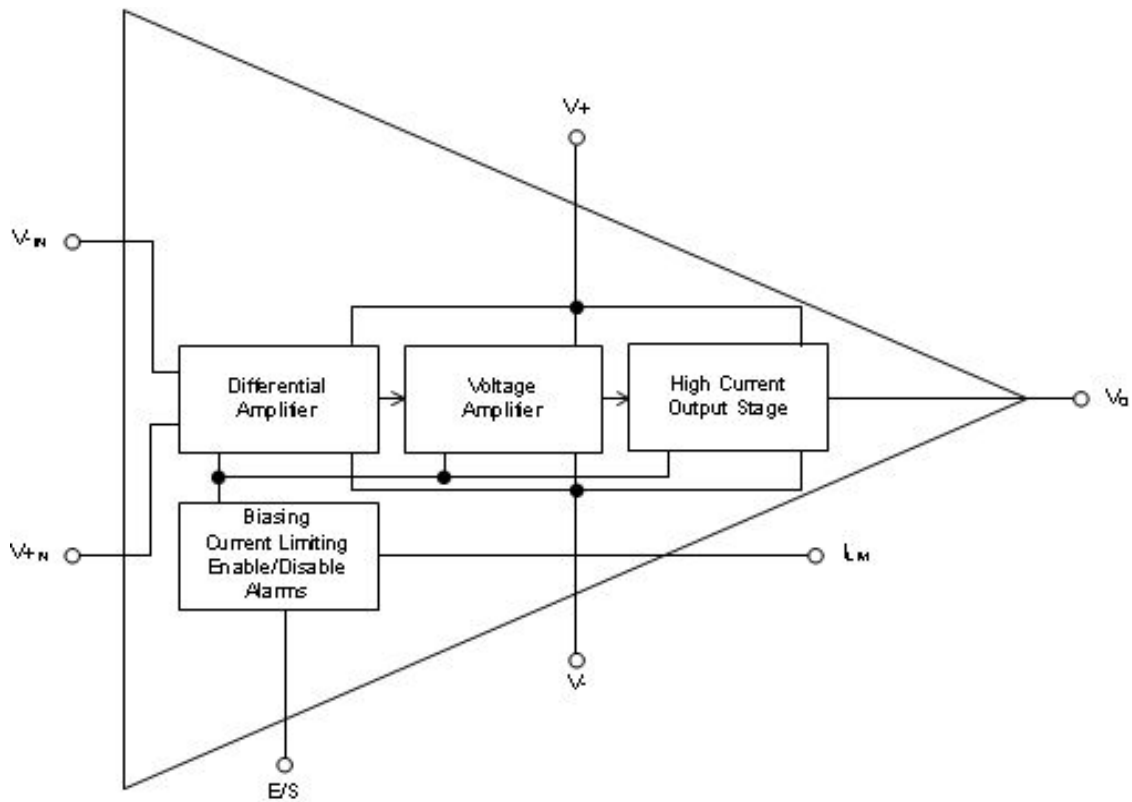
A multisim of the analog design portions with appropriate testing data.

An examination into the noise caused by the high frequency environment of the project with a note of steps taken to reduce this factor.

PCB layout of analog portions of the design.

A final PCB board with all components attached and appropriate testing for functionality and reliability.

3 Design



3.1 PREVIOUS WORK/LITERATURE

There are no similar products that can replace our circuit. This circuit is designed specifically for Dr. Bigelow's research project. Our reference literature is Microelectronic Circuits by Sedra and Smith, along with datasheets for the individual products such as the multiplexer or op-amps. In addition we have the documentation from a previous Senior Design group that was unable to get their project fully operational. Although we have decided to rebuild from scratch, and not use the previous senior design group's design. Listed below are our reference documentation for our hardware

Power Amplifier - <http://www.ti.com/lit/ds/symlink/opa548.pdf>

Launchpad Library - http://e2e.ti.com/cfs-file/_key/communityserver-discussions-components-files/171/0410.DPLib.pdf [Download link]

Filter Amplifier -

http://www.analog.com/media/en/technical-documentation/data-sheets/ADA4891-1_4891-2_4891-3_4891-4.PDF

3.2 PROPOSED SYSTEM BLOCK DIAGRAM



3.3 ASSESSMENT OF PROPOSED METHODS

For the low-pass filter segment our design choice was made based on the needed simple functions of the low-pass filter which was simply a cutoff frequency of 1.5Mhz and the design was selected based upon it's ability to do that as well as a few methods for making other portions of the design simpler. With an active low-pass filter with a gain of one it makes the amplification segment's planning easier as we do not need to know the voltage drop caused during the filter. The ADA4891-3 was chosen as our op amp based on the needed slew rate at the high frequencies that our filter will be receiving and outputting. As such the necessary 167v/us slew rate was met while all other parameters of the op amp only needed to be observed as a secondary thought. The control of the cutoff frequency for our design can be performed by simple resistors and capacitors in the testing phase while more accurate resistor values may be required for a final product.

For the power amplifiers there a number of types of power amplifier circuits that could fit our specifications. An original thought was to use two separate amplifiers to first increase the voltage of our signal, then another amplifier to increase our current output. The high-voltage OPA548 satisfies both needs and has an easy to set current limiter so we can control gain and current output from 0-5 amps using common resistors. The TI Launchpad we've chosen has a very functional processor, it has the speed, the digital signal library support, and many outputs to satisfy our digital signal splitting and analog conversion needs.

3.4 VALIDATION

Confirmation of design ideas will done through a mixture of Simulink, PSPICE, and physical testing. Each will be used depending on the needs of the individual segment of the project. Due to limitations in PSPICE models, the ability to generate a high enough frequency input, and other limitations certain methods will not always work but depending on the situation close approximations will be used instead.

Our original intention was to begin testing our components together soon after we received them. However, when it came time to order our parts we soon discovered that

through-hole type op-amps weren't as common as we students imagined. We wouldn't be able to simply plop the components down into a breadboard and start testing. Either a surface-mount adapter would need to be made, or a rough PCB would have to be made in order for the components to come together.

We will also need sometime to learn the libraries of the Launchpad before any sort of DSP validation can be done. In theory the launchpad can do everything we want it to and more, it's just a matter of programming and processor that is unfamiliar to all of us.

4 Project Requirements/Specifications

4.1 FUNCTIONAL

Functional - Tested

- Input 50Mhz signal split into two 25Mhz signals.
- Signals run successful through low pass filter and output waveform appears sinusoidal in nature.
- Signal created by a function generate to mimic the low pass filter output has been amplified to the required output signal.

Functional - Untested

- DAC of 25 Mhz
- Launchpad feeding input to filters
- Filters feeding into power amp
- Power amp output to Dr. Bigelow's sensors

4.2 NON-FUNCTIONAL

Our first PCB design is about to be complete. It contains two separate grounding planes, mount points for our op-amps, and many resistors. This design will need to be created to have a complete working version capable of connecting to Dr. Bigelow's current setup. Once we test it all together, we will be able to start creating a list of changes to make and begin creating modifications to our design. We expect to have several PCB versions created and tested before the end of our second semester.

- Effective protection from circuit noise due to high frequency signals.
- Most cost effective method selected.
- Capable of being repeated for scalability to suit operational needs.
- Protection against possible high current bursts.
- Considerations for heat dissipation concerns.

5 Challenges

From a feasibility perspective there is no doubt that the project is possible, however, the main question is one of feasibility with the available resources of a student. With our project divided into three main components, the DAC Multiplexer, the filters, and the amplifiers it makes sense to look at the project feasibility from the perspective of each of these individual parts.

Firstly the DAC Multiplexer which is currently being fulfilled using the TI Launch Pad Piccolo C2000 at a cost of 17.70 per unit. The final product that our drive circuitry is going into needs 128 channels for the DAC multiplexer (the C2000 only has 8) making the final cost of all 128 channels around 284 dollars which, while cost prohibitive for

our particular budget, is not an unreasonable amount of money to spend on the product being developed in this case. Issues with the C2000 are still being examined with programming work currently being done to determine whether it can without a doubt function as needed with the correct phase control. In addition concerns exist as to whether the C2000 will be able to produce the proper voltage output with all 8 channels simultaneously. Failing that proper amendment can be made to the other two portions to accommodate so long as there is some voltage output coming from each of the 8 channels. At the current moment this solution to the problem of the DAC multiplexer can be deemed sound and feasible.

Second the filters which are the most simple portion of the drive circuitry. The 170v/us slew rate of the ADA4891-3 op amp provides all the necessary requirements for the simple unity gain low-pass filter that is being used in this portion so provided there are no massive changes needed in the low-pass filter circuit the current design should prove effective and without issue. With a cost of 1.39 per unit this choice is certainly no issue in terms of costs as well.

Finally there is the matter of the amplifiers which is currently being performed by the OPA548T op amp with a cost of 15.01 per unit which when considering for the full model would require 128 of this could be considered the most expensive portion of the design. From a feasibility perspective the part meets all the necessary requirements to perform the necessary amplification of the signal and as such can be considered feasible. Testing of the circuit design is still in the process and as such cannot be considered sound but provided changes need to be made to the circuit the current op amp should be feasible with any foreseeable changes.

As such from a cost perspective for the device it could be said that is expensive to implement all channels in a senior design project. However given the nature of what the drive circuitry is being used for and the cost associated with machines that perform similar functions it could be said that this is far more cost efficient. Other challenges that include concerns with noise due to the high frequency nature of our signals and the necessary load requirements stipulated in our initial parameters however we feel that the feasibility of our design looks well.

6 Timeline

6.1 FIRST SEMESTER

- The initial phase of the project started with group discussions on design and individual research into individual portions of the projects functions. Each member's individual area of focus for the semester is listed below.
 - Miguel Mondragon - Team leader: Reports, emails, and filter design.
 - Zechariah Pettit - Webmaster: Website design and amplifier design.
 - Honghao Liu - Key Concept Holder and DAC Multiplexer design.
- March 14th - Initial designs and parts decided upon.
- March 21st - Initial parts order for testing.
- April 10th - Initial designs tested and redesigns begin. Initial PCB design begins.
- April 23rd - Primary design for PCB finalized. Sent to Dr. Bigelow for approval.
- Summer of 2016 - Small scale design edits as desired and small-scale PCB design.

6.2 SECOND SEMESTER

Plans for the second semester are dependent on needs and constraints set forth by the previous semester all current goals and deadlines are below.

- September 1st - PCB test board ordered.
- October 15th - All final designs, parts, and constraints tested within the high frequency environment set forth by the project specifications.
- November 15th - Final PCB layout determined and ordered. Following it's arrival further testing to determine final functionality will be done.

7 Conclusions

The project's overall goal is to take a number of 50Mhz signals and split them into two separate 25Mhz signals with a user determined phase control. This is followed by a low-pass filter with a gain of one and a cutoff frequency of 1.5MHz. Finally there is a large amount of power amplification that needs to occur as the final output signal is sent to the next part of the device.

Currently our project is in the stage of assembling the elements of the overall design so that a mock up can be constructed and tested. This includes PCB test boards, breadboard circuits, and the initial stages of programming in the case of the TI Launch Pad.

8 References

Microelectronics by Sedra and Smith

Senior Design Group, DEC1301 Design Documentation

9 Appendices

[ADA4891-3 Op Amp](#)

[OPA548 Op Amp](#)

[ADA4522-2 Op Amp](#)

[LAUNCHXL-F28027 C2000 Piccolo LaunchPad](#)